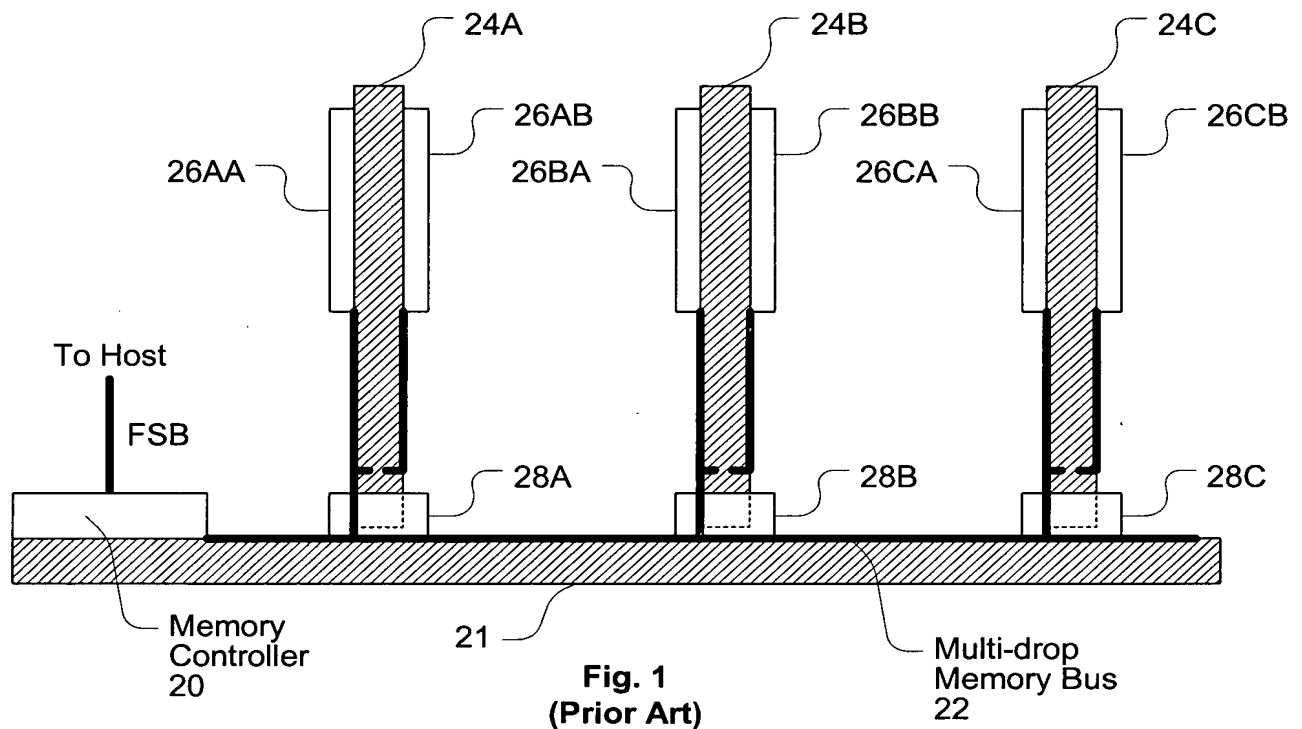


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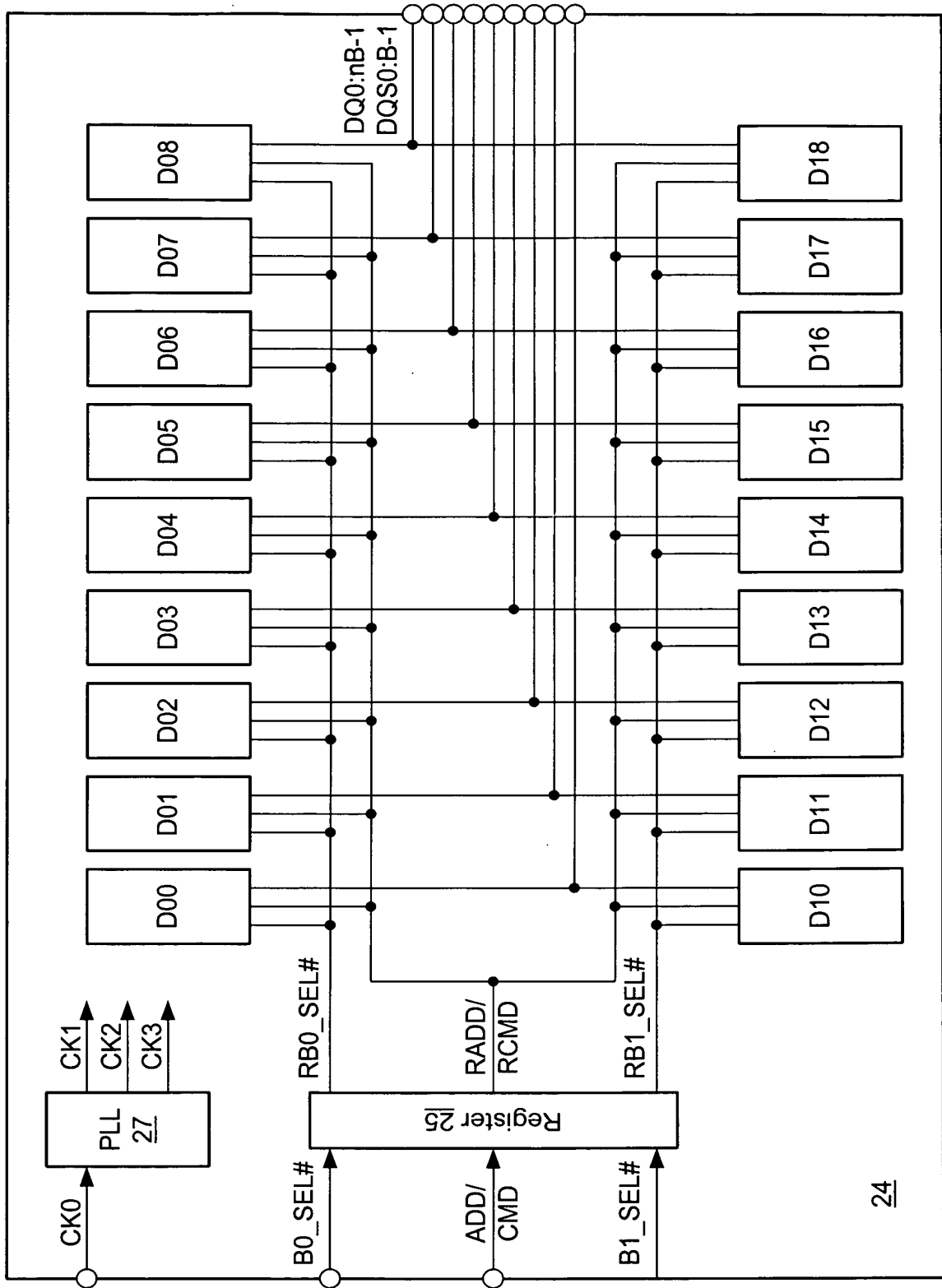


Fig. 2
(Prior Art)

FIG. 3 is a timing diagram of a memory device in accordance with the present invention. The diagram shows the relationship between various signals and time intervals T1 through T9.

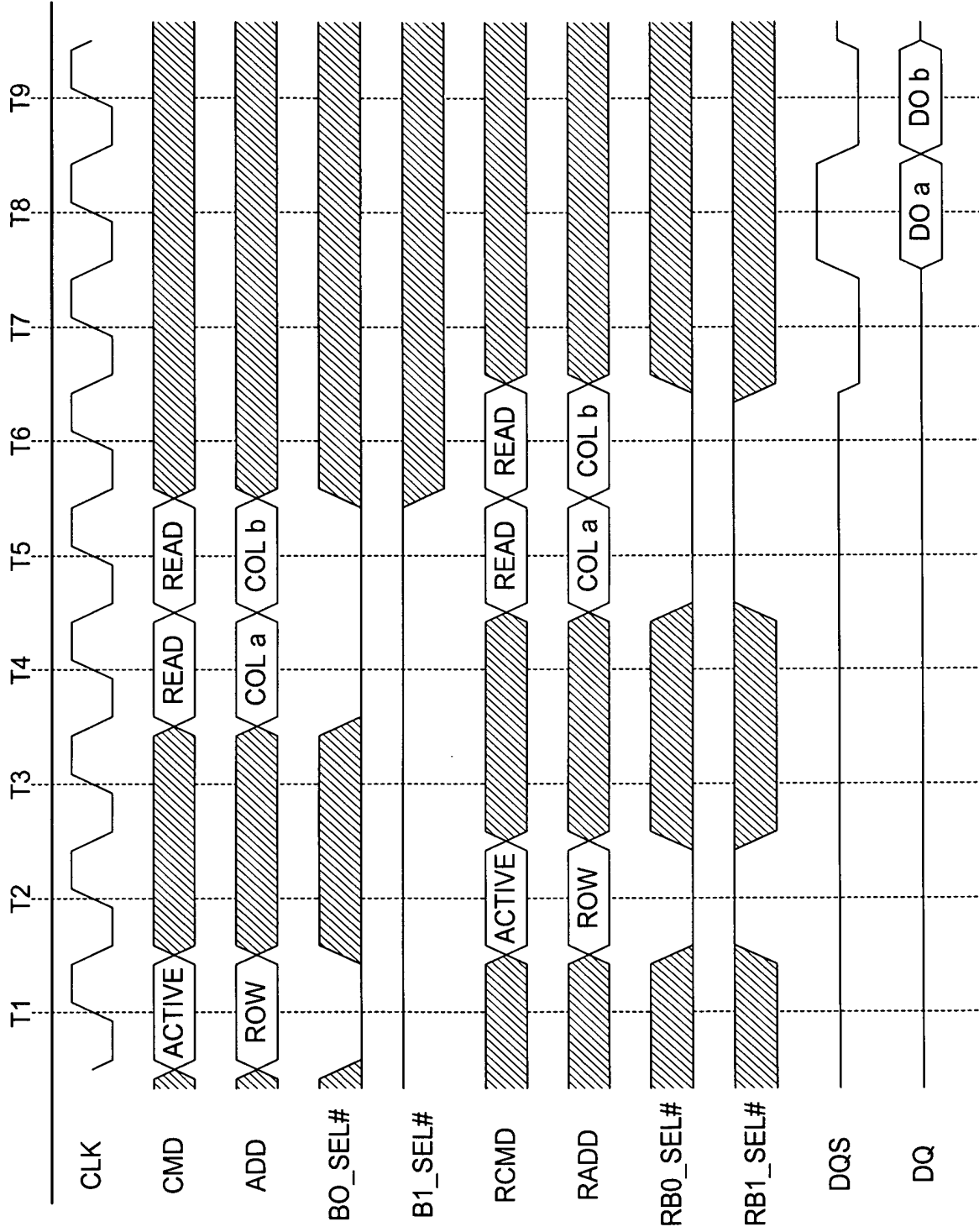


Fig. 3
(Prior Art)

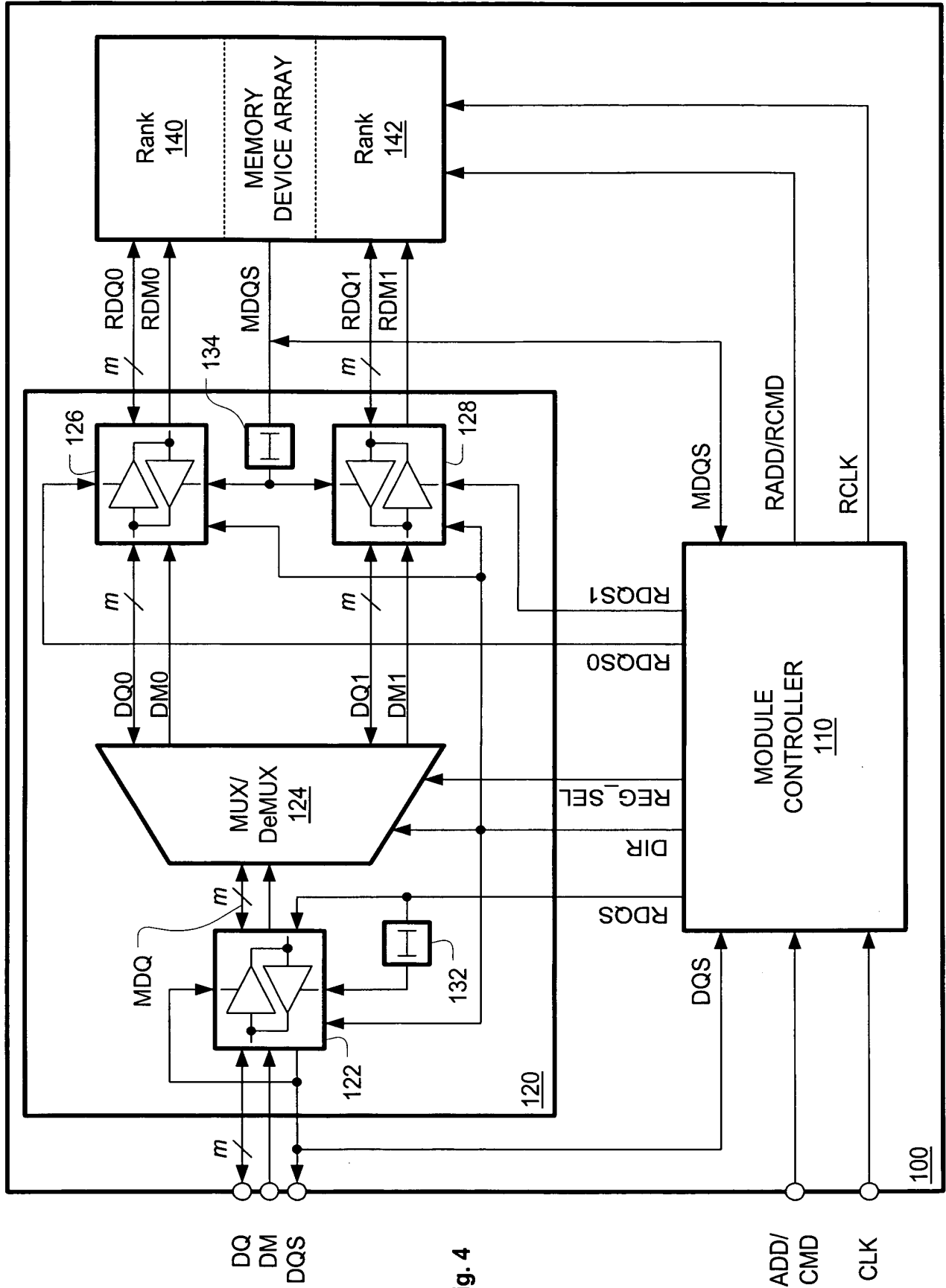
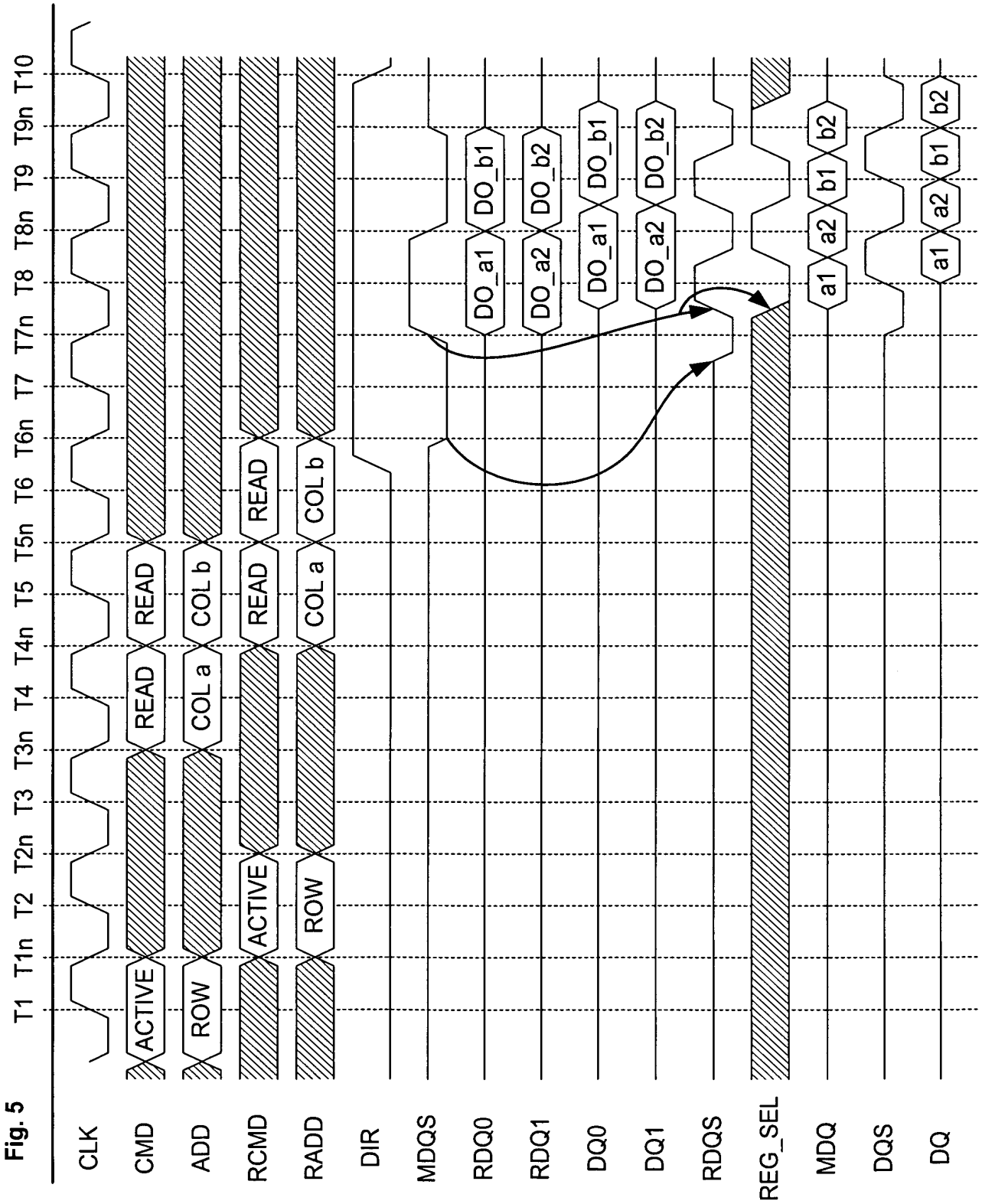


Fig. 4



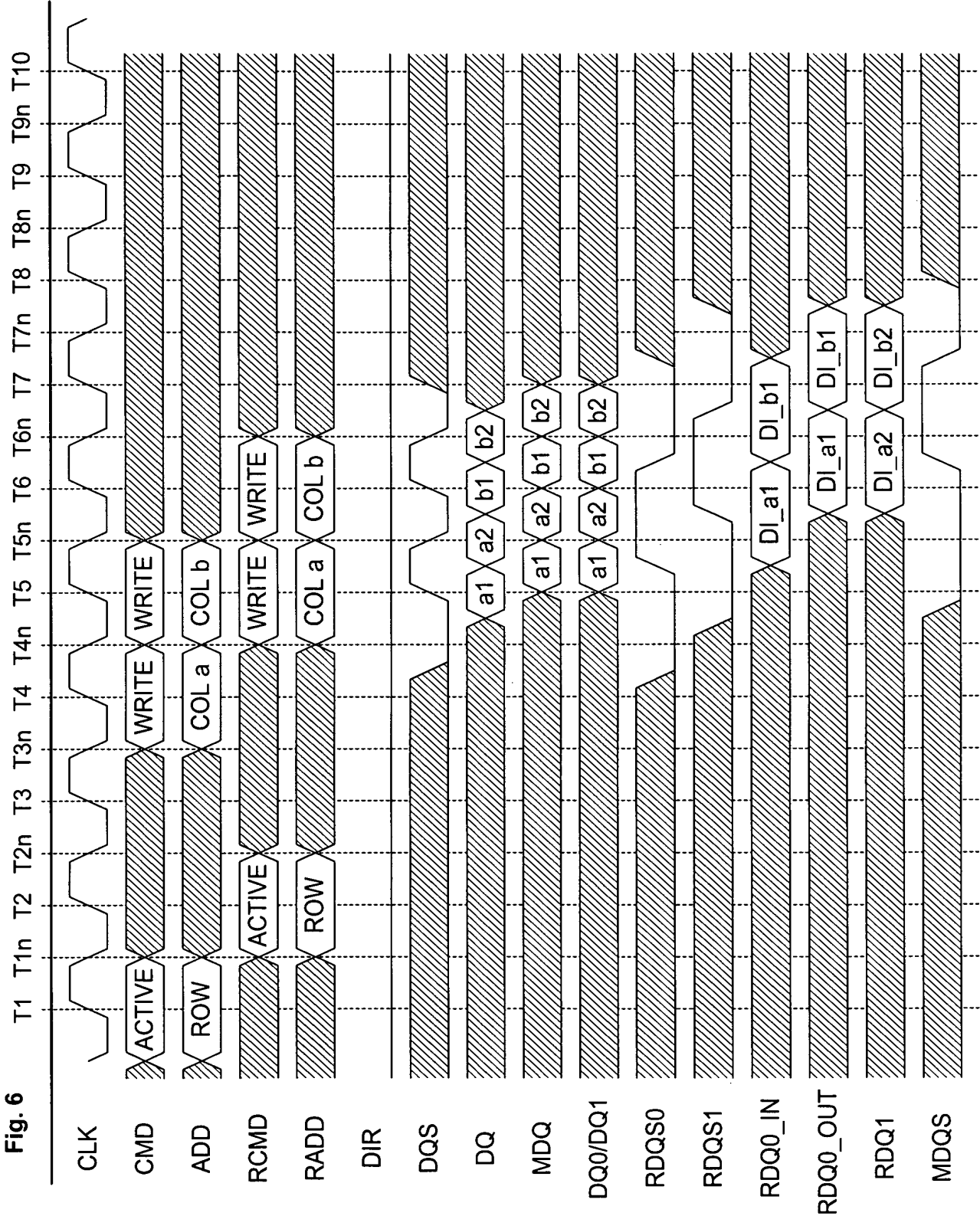


Fig. 7

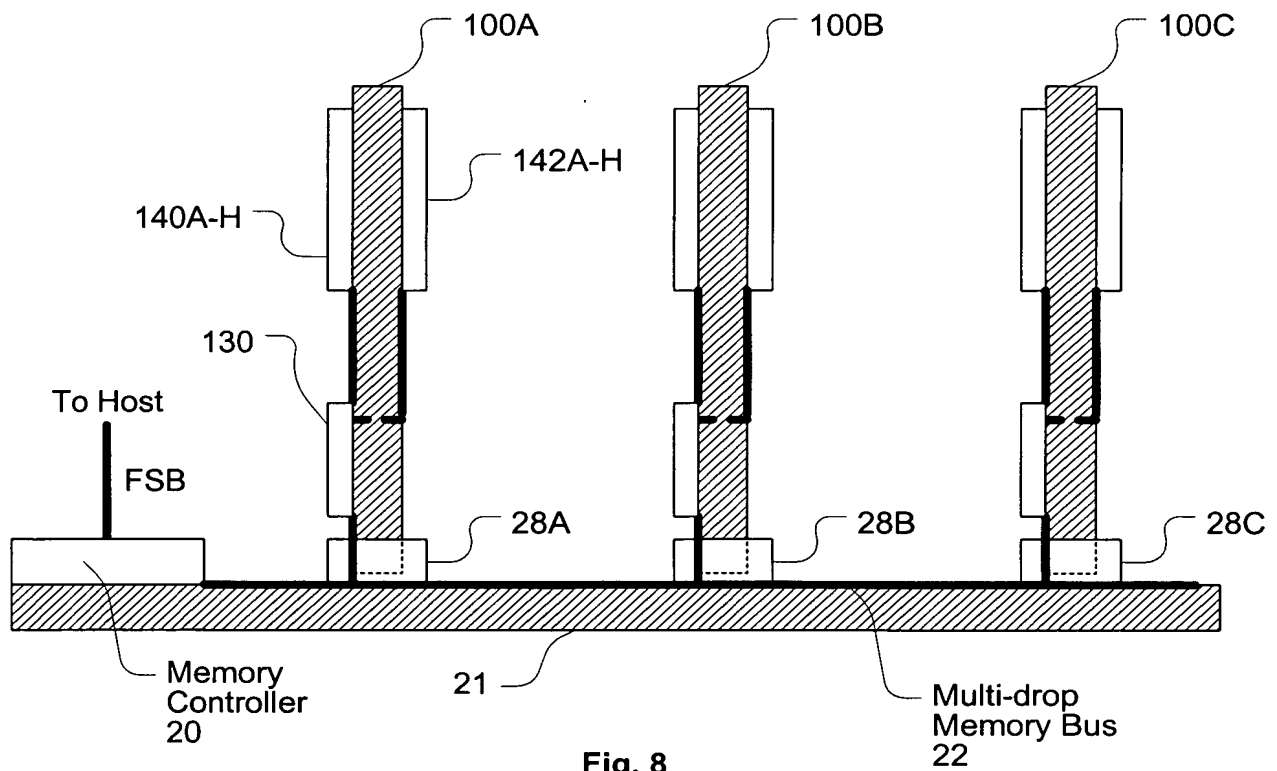
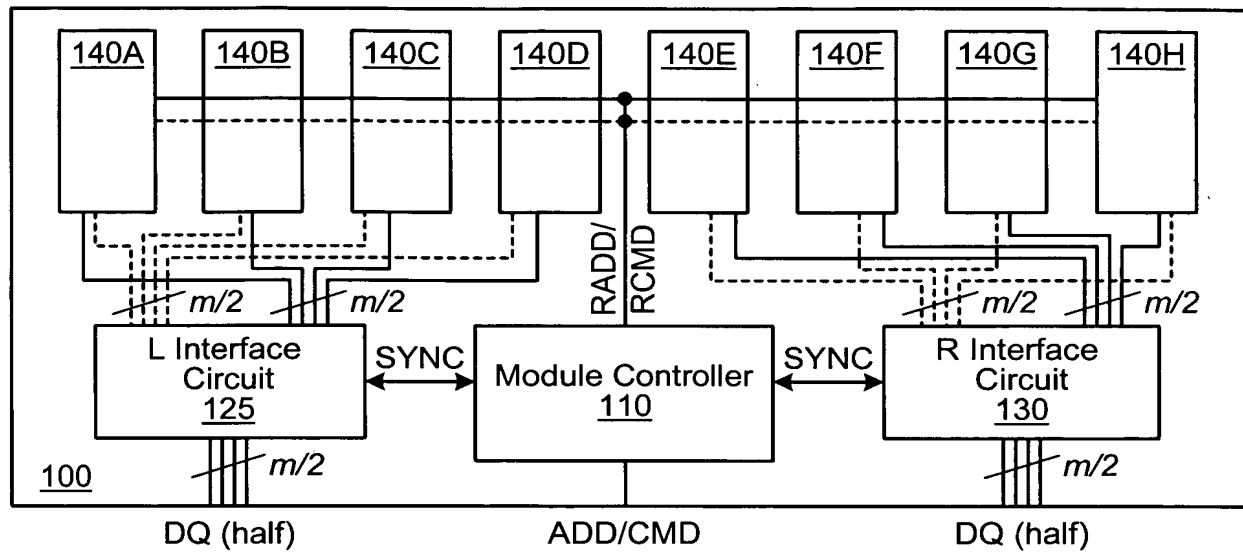


Fig. 8

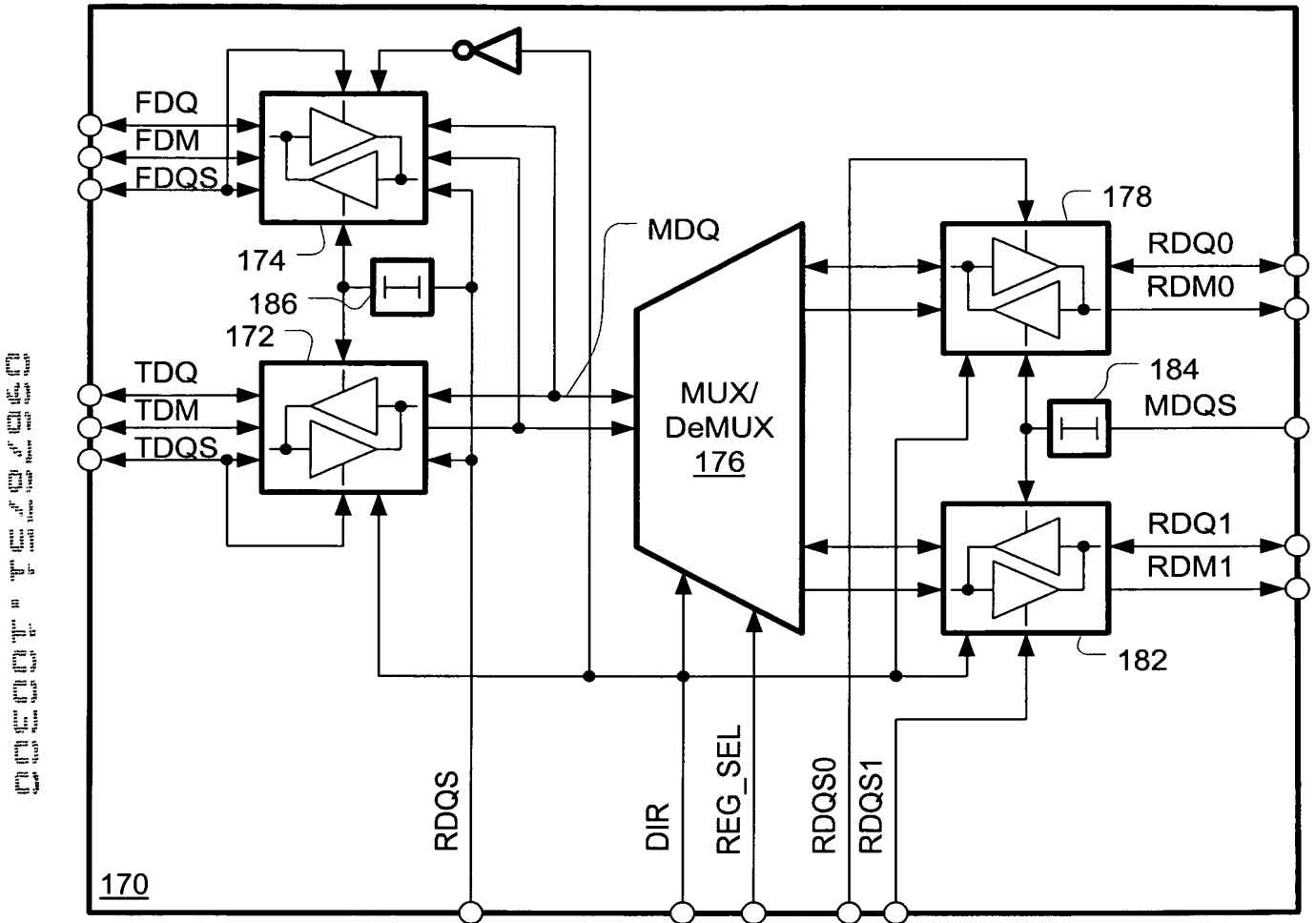
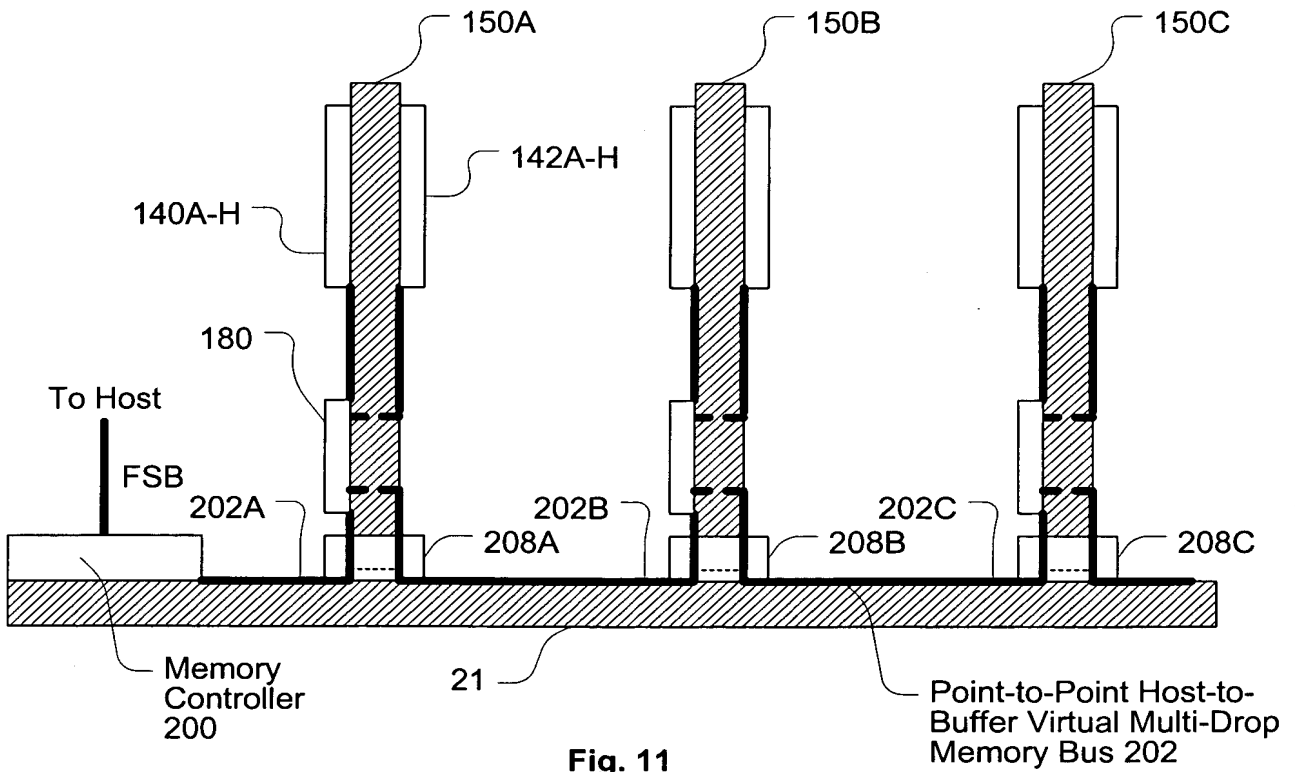
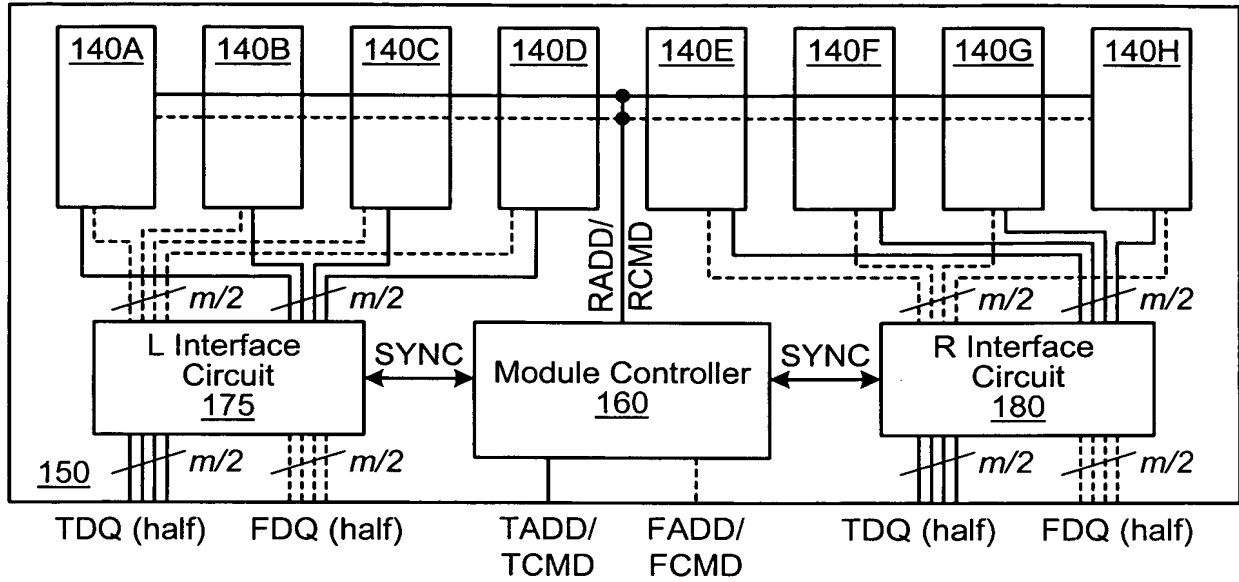


Fig. 9

Fig. 10



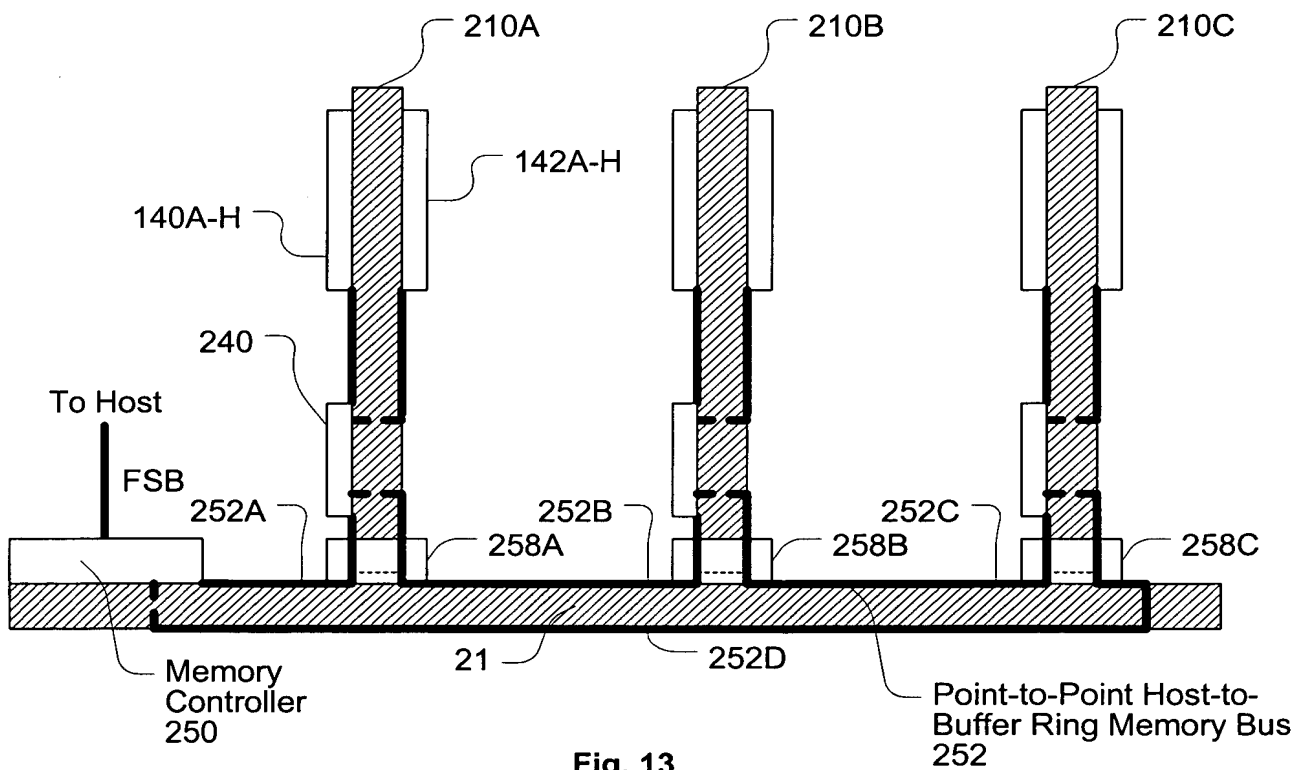
[illegible]

Fig. 13